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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/751,307	12/31/2003	Mohamed Soufi	03226.356001; SUN040029	8806

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EXAMINER	
OCHOA, JUAN CARLOS	
ART UNIT	**PAPER NUMBER**
2123	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/20/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/751,307	SOUFI ET AL.	
	Examiner	Art Unit	
	Juan C. Ochoa	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 January 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5,7-12 and 14-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,7-12 and 14-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. The amendment filed 1/3/07 has been received and considered. Claims 1–5, 7–12, and 14–22 are presented for examination.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to

consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims 1–5, 7–12, and 14–22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fujiwara et al., (Fujiwara hereinafter), U.S. Patent 6,510,541 taken in view of Tseng et al., (Tseng hereinafter), U.S. Patent 6,009,256

6. As to claim 1, Tseng discloses a method for providing verification for a first simulation image, comprising: producing an optimized image (see col. 22, lines 9–11); simulating the optimized image (see Fig. 2, item No. 135); simulating the second simulation image to gather simulation data (see Fig. 2, item No. 145); debugging the first simulation image using simulation data (see col. 9, lines 61–67 and Fig. 2, item No. 115); and verifying one selected from a group consisting of the optimized image and the second simulation image (see col. 16, lines 62–64).

7. While Tseng discloses a method for providing verification for a first simulation image, Tseng fails to expressly disclose removing nodes from the first simulation image to produce an optimized image and an optimized nodes image; invoking the optimized nodes image; and reconstructing a second simulation image using the optimized image and the optimized nodes image.

8. Fujiwara discloses removing nodes from the first simulation image to produce an optimized image (see col. 16, lines 59–64 and/or col. 19, lines 23–25) and an optimized nodes image (see "optimization model" in col. 18, line 63 to col. 19, line 9 and Fig. 29);

invoking the optimized nodes image (see col. 19, lines 26–29) if debugging is selected; and reconstructing a second simulation image using the optimized image and the optimized nodes image (see col. 19, lines 20–23).

9. As per the definition "unobservable nodes (or not directly observable nodes), e.g., a scan chain and a large amount of circuitry that does not directly affect verification output" (see application description page 9, paragraph [0035]), Examiner interprets "removing nodes from the first simulation image to produce an optimized image" as Fujiwara's "although the module MD is included in the data, it does not influence the simulation results at all" (see col. 19, lines 10–25).

10. As per the definition "redundant logic" (see application description page 9, paragraph [0035]), Examiner interprets "removing nodes from the first simulation image to produce an optimized image" as Fujiwara's "circuit change part 522 deletes the processing 2a and the conditional sentence in the control description 2" (see col. 17, lines 3–12).

11. As per the definition "Nodes that are optimized out of a simulation image are referred to as "optimizable nodes" (see application description page 9, paragraph [0035]), Examiner interprets "to produce an optimized image" as Fujiwara's "such a circuit for simulation that can automatically generate a simulation model detaching the module MD is generated" (see col. 19, lines 23–25).

12. Tseng and Fujiwara are analogous art because they are both related to verification of electronic systems.

13. Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to utilize the teachings of Fujiwara in the method of Tseng because Fujiwara provides a database for design of an integrated circuit where data usable for system verification is stored in a flexibly utilizable state (see col. 1, lines 62–67), and as a result, Fujiwara reports the following improvements over his prior art: reduction in simulation speed by reducing instances of optimized away unused modules in memory and their signal changes (see col. 19, lines 10–31).

14. As to claim 2, Fujiwara discloses a method wherein the first simulation image and the second simulation image comprise a register transfer level design (see "RT layer" in Fig. 4).

15. As to claim 3, Fujiwara discloses a method wherein debugging comprises comparing a reference value to a value of a corresponding register transfer level design component of at least one selected from the group consisting of the optimized image and the second simulation image (see col. 17, lines 44–67 and "signals" in and Fig. 25 and Fig. 26).

16. As to claim 4, Fujiwara discloses a method wherein the optimized nodes image comprises at least one node selected from the group consisting of a redundant node, an unobservable node, and a dangling node (see redundant and/or dangling in col. 19, lines 10–19 and Fig. 30).

17. As to claim 5, Fujiwara discloses a method wherein the optimized nodes image comprises a list of optimized nodes and information about how to compute the

optimized nodes image from the optimized image (see "hierarchy expansion part" in col. 18, lines 1–12 and Fig. 26, item No. 524).

18. As to claim 7, Tseng discloses a method further comprising: isolating and eliminating a bug in the first simulation image using simulation data (see col. 9, lines 61–67 and Fig. 2, item No. 115).

19. As to claims 8–12 and 14, these claims recite a computer system for performing the method of claims 1–5 and 7. Tseng discloses a system (see col. 1, lines 8–11) for performing a method that teaches claims 1–5 and 7. Therefore, claims 8–12 and 14 are rejected for the same reasons given above.

20. As to claim 15, Tseng discloses a system (see col. 1, lines 8–11) for verifying a first simulation image, comprising: an optimizer tool (see col. 22, lines 9–11); a test vector (see Fig. 3, item No. 235) providing an input signal value for a component in at least one selected from the group consisting of the optimized image and a second simulation image (see Fig. 3, item No. 255); wherein the testbench provides functionality to verify at least one selected from the group consisting of the optimized image and the second simulation image using the test vector (see col. 16, lines 62–64). While Tseng discloses a system for providing verification for a first simulation image, Tseng system lacks an optimizer tool providing functionality to optimize the second simulation image into an optimized image and an optimized nodes image and a reconstructor tool of a testbench providing functionality to reconstruct the second simulation image using the optimized image and the optimized nodes image, if

debugging is selected. Fujiwara discloses an optimizer tool providing functionality to optimize the second simulation image into an optimized image and an optimized nodes image (see "optimization model" in col. 18, line 63 to col. 19, line 9 and Fig. 29) and a reconstructor tool of a testbench providing functionality to reconstruct the second simulation image using the optimized image and the optimized nodes image (see col. 19, lines 20–23), if debugging is selected.

21. As to claims 16–20, these claims recite a computer system for performing the method of claims 1–5. Tseng discloses a system (see col. 1, lines 8–11) for performing a method that teaches claims 1–5. Therefore, claims 16–20 are rejected for the same reasons given above.

22. As to claim 21, Tseng discloses a method wherein producing the optimized image comprises reorganizing an original logic of the first simulation image into a simulation-friendly implementation. (See "reorganized" in specification's page 10, paragraph [0037] as "the circuit change part 522 deletes the processing 2a and the conditional sentence in the control description 2" in col. 17, lines 9–12, and Fig. 24).

23. As to claim 22, Tseng discloses a method wherein producing the optimized image comprises reorganizing an original logic of the first simulation image into a simulation friendly implementation. (See "reorganized in specification's page 10, paragraph [0037]" as "the circuit change part 522 deletes the processing 2a and the conditional sentence in the control description 2" in col. 17, lines 9–12, and Fig. 24).

Response to Arguments

24. Applicant's arguments filed 1/3/07 have been fully considered but they are not persuasive.

25. Regarding the claim objections, the amendment corrected all deficiencies and the objections are withdrawn.

26. Regarding the rejections under 101, the amendment corrected all deficiencies and the rejections are withdrawn.

27. Regarding the rejection under 103.

28. Applicant's arguments, (see page 8, last 2 paragraphs, page 9, and page 10, 1st paragraph), have been considered, but they are not persuasive. Examiner has further elaborated such Fujiwara disclosures in the instant rejection.

29. Applicant's argument, (see page 9, 2nd paragraph), has been considered, but it's not persuasive. While the Examiner previously relied upon Fujiwara's (col. 19, lines 23–25) as disclosing "invoking the optimized nodes image", which applicant's arguments address, the Examiner now relies upon Fujiwara's (col. 19, lines 26–29) to support the rejection. Therefore, the Examiner now relies upon elements present in Fujiwara's (col. 19, lines 26–29) to support "invoking the optimized nodes image". Examiner has further elaborated such Fujiwara disclosure in the instant rejection.

30. Therefore it is the Examiners position that the cited references do anticipate the claims and the rejections are maintained.

Conclusion

31. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

32. Examiner would like to point out that any reference to specific figures, columns and lines should not be considered limiting in any way, the entire reference is considered to provide disclosure relating to the claimed invention.

33. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Juan C. Ochoa whose telephone number is (571) 272-2625. The examiner can normally be reached on 7:30AM - 4:00 PM.

34. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul Rodriguez can be reached on (571) 272-3753. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

35. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

*** JO 3/14/07

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3/15/07